

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. US Patent No. 6081878 (herein after referred to as Estakhri) in view of Klein et al. US Patent No. 5671439 (herein after referred to as Klein).

Regarding claim 1, Estakhri describes a data write-in method for a flash memory, wherein the flash memory comprises at least two flash chips (**flash memory chips 670 and 672 of Fig. 6 (column 6, lines 23 – 52)**) and a controller (**controller 510 of Fig. 6 (column 6, lines 23 – 52)**). While Estakhri does describe one particular interleaving method (**Fig. 13**), Estakhri does not specifically describe the method comprising: partitioning physical blocks in the at least two flash chips such that the physical blocks in one of the at least two flash

chips have odd logical block addresses and the physical blocks in another one of the at least two flash chips have even logical block addresses; the controller receiving a data write-in instruction and analyzing a beginning logical address for writing from the received data write-in instruction; the controller obtaining the logical block address needed to be written according to the analyzed beginning logical address; the controller determining a parity of the obtained logical block address, and selecting one flash chip from the flash chips according to the determined parity of the logical block address; the controller directing a first programming or erasing instruction to the physical blocks corresponding to the obtained logical block address in the selected flash chip; the controller detecting whether said another one flash chip needs to be programmed or erased while the first programming or erasing instruction are being processed; if programming or erasing is needed in said another one flash chip, the method further comprises: the controller directing a second programming or erasing instruction to said another one flash chip of at least two flash chips.

Klein describes a data write-in method for a flash memory (**It will be appreciated that other physical mass storage devices may be used...Examples include...flash memories...(column 14, line 66- column 15, line 5)**), wherein the flash memory comprises at least two flash chips (**Drive A and Drive B of FIG. 2**), and the method comprises: partitioning physical blocks in the at least two flash chips such that the physical blocks in one of the at least two flash chips have odd logical block addresses and the physical blocks in

another one of the at least two flash chips have even logical block addresses (means for alternately transferring even-numbered blocks of physical sectors between the on-board memory of the first drive and the main processing system and transferring odd-numbered blocks of physical sectors between the on-board memory of the second drive and the main processing system (column 4, lines 36 - 41)); receiving data write-in instruction and analyzing a beginning logical address for writing from the received data write-in instruction (The preferred routine preferably receives as input a starting logical sector START (column 8, lines 16 - 18). Retrieve xfer command 102 of FIG. 2. Furthermore over the course of time that this invention is operating it will retrieve a plurality of xfer commands); obtaining the logical block address needed to be written according to the analyzed beginning logical address; determining a parity of the obtained logical block address, and selecting one flash chip from the flash chips according to the determined parity of the logical block address (Starting sector on drive A? 132 of FIG. 2); directing first programming or erasing instructions to the physical blocks corresponding to the obtained logical block address in the selected flash chip (Starting sector on Drive A 132 of FIG. 2 following either YES path to Drive A Ready? 136 or NO path to Drive B Ready? 146); detecting whether said another flash chip needs to be programmed or erased while the first programming or erasing instruction are being processed (More? 142 of FIG. 2. For example first-in/first-out (FIFO) register and/or direct memory access

(DMA) circuitry may be used to temporarily store information related to a non-selected physical device while a transfer is occurring between a selected physical device and the host computer memory. Then once the transfer is complete on the selected device the information from the non-selected device may be burst into or from the main memory at an extremely high rate by the FIFO and/or DMA circuitry (column 8, lines 1 - 10); if programming or erasing is needed in in said another one flash chip, the method further comprises: directing a second programming or erasing instruction to said another one flash chip of at least two flash chips (More? 142 of FIG. 2 following YES path to Drive B Ready? 146**).** Klein essentially describes a specific mapping method that allows for faster data transfer by sending odd logical blocks to one memory and even logical blocks to a different memory. The mapping method could obviously be applied to the flash memory configuration of Estakhri where the controller would direct access between the two flash chips.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the interleaving method described by Klein in the flash memory of Estakhri because Klein explains that using this method overall sustainable data transfer rates may be improved by requesting the physical devices to begin access at substantially the same time (**column 3, lines 14 - 18**).

Regarding claim 3, Estakhri in view of Klein describe the data write-in method for a flash memory according to claim 1 (**see above**). Estakhri does not

specifically describe wherein if said another one flash chip does not need to be programmed or erased, the method further comprises: judging whether the processing of the first programming or erasing instruction is finished.

Klein describes wherein if the other flash chip does not need to be programmed or erased, the method further comprises: judging whether the processing of the first programming or erasing instruction is finished (**No path from More? 142 of Fig. 2**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the interleaving method described by Klein in the flash memory of Estakhri because Klein explains that using this method overall sustainable data transfer rates may be improved by requesting the physical devices to begin access at substantially the same time (**column 3, lines 14 – 18**).

Regarding claim 6, Estakhri in view of Klein describe the data write-in method for a flash memory according to claim 1 (**see above**). Estakhri does not specifically describe wherein the analyzing further comprises: obtaining the number of sectors needed to be written from the data write-in operation instruction.

Klein describes wherein the analyzing further comprises obtaining the number of sectors needed to be written from the data write-in operation instruction (**Calculate starting and total sectors for drives A & B 200 of Fig. 2**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the interleaving method described by Klein in the flash memory of Estakhri because Klein explains that using this method overall sustainable data transfer rates may be improved by requesting the physical devices to begin access at substantially the same time (**column 3, lines 14 – 18**).

Regarding claim 7, Estakhri in view of Klein describe the data write-in method for a flash memory according to claim 6 (**see above**). Estakhri does not specifically describe that the analyzing further comprises: judging whether the data write-in instruction has been finished by subtracting a number of written sectors from a number of sectors needed to be written.

Klein describes that the analyzing further comprises: judging whether the data write-in instruction has been finished by subtracting a number of written sectors from a number of sectors needed to be written (**338 and 340 of Fig. 5(b)**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the interleaving method described by Klein in the flash memory of Estakhri because Klein explains that using this method overall sustainable data transfer rates may be improved by requesting the physical devices to begin access at substantially the same time (**column 3, lines 14 – 18**).

Response to Arguments

4. In response to applicant's argument that there is no teaching, suggestion, or motivation to combine the references, the examiner recognizes that obviousness may be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), and *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007). In this case, Estakhri and Klein are in the same field of endeavor, methods of writing data to memory. As explained in the previous office action, it is believed that the combination of Estakhri and Klein would benefit from Klein's method of interleaved writing between two storage devices which can improve overall sustainable data transfer rates by requesting the physical devices to begin access at substantially the same time (Klein, column 3, lines 14 – 18).

5. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., simultaneously reading/writing) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Examiner further points out that the term "simultaneously" only seems to appear once in the background of the specification (see page 1 of the originally filed

specification) and not the detailed description. Applicant's own description seems to point more to a method of starting A and subsequently starting B while A is still being worked on (after being started) as opposed to starting A and B simultaneously.

6. Applicant argues, with respect to claim 1, that according to Klein during a transfer phase drive B must wait until operation on drive A is finished and vice versa. Examiner points out that Klein mentions that first-in/first-out (FIFO) registers and/or direct memory access (DMA) circuitry may be used to temporarily store information related to a non-selected physical device while a transfer is occurring between a selected physical device and the host computer memory (column 8, lines 3 – 12). While one device is in the transfer phase the other device can be in the access phase such that each device is being utilized during the others processing.

7. Applicant argues, with respect to claim 1, that it is impossible for the system of Klein to transfer data simultaneously to drive A and drive B because all data is transferred through "Data Path" 70. Examiner first points to the use of "simultaneously" in the arguments and refers to the response related to that above. Furthermore, Data Path 70 shows how data gets to FIFOs A and B which each have their own data connection to the drives via DATA0 73 and DATA1 75 respectively. Examiner points out that Klein mentions that first-in/first-out (FIFO) registers and/or direct memory access (DMA) circuitry may be used to temporarily store information related to a non-selected physical device while a transfer is occurring between a selected physical device and the host computer memory (column 8, lines 3 – 12). While one device is in the transfer phase the other device can be in the access phase such that each device is

being utilized during the others processing. For example, while data is being transferred from the PCI BUS 61 to FIFO A via DATA PATH 70, data can also be transferred from drive B to FIFO B via DATA1 75. Column 17, lines 16 – 36 further describes the operation using the FIFOs.

8. Applicant argues, with respect to claim 1, that due to inherent characteristics of the flash as mentioned in the Background of the subject application, the solution of Klein is not applicable to the flash. As explained in the rejections and responses above, Examiner believes that Klein teaches a method of accessing memory that reads on the method presented in the claims. Klein further explains that the type of memory device used may be flash memory. Therefore, Klein's method of accessing the memory is applicable to flash.

9. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., not needing to revise or improve the hardware of the host) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

10. Applicant argues, with respect to claims 3, 6 and 7, that claims depending from claim 1 should also be allowable for the same reasons. Examiner refers to rejections and responses above as to why those claims are not allowable.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RALPH A. VERDERAMO III whose telephone number is (571)270-1174. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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